



(19) **United States**
(12) **Patent Application Publication**
PARK

(10) **Pub. No.: US 2014/0118323 A1**
(43) **Pub. Date: May 1, 2014**

(54) **ORGANIC LIGHT EMITTING DISPLAY**

(52) **U.S. Cl.**

(71) Applicant: **SAMSUNG DISPLAY CO., LTD.,**
Yongin-City (KR)

CPC **G09G 3/3291** (2013.01)

USPC **345/212; 345/82**

(72) Inventor: **Sung-Cheon PARK, Yongin-City (KR)**

(57) **ABSTRACT**

(73) Assignee: **SAMSUNG DISPLAY CO., LTD.,**
Yongin-City (KR)

An organic light emitting display includes: a plurality of pixels coupled to scan lines and data lines; a scan driver that supplies a scan signal to the pixels through the scan lines according to a predetermined scan frequency; a data driver that supplies a data signal to the pixels through the data lines; and a first switching regulator that supplies a first voltage to the pixels and has a changeable switching frequency. In the organic light emitting display, the switching frequency of the first switching regulator is changed while avoiding the scan frequency of the scan driver. Accordingly, it is possible to provide an organic light emitting display which can improve power conversion efficiency and reduce a flicker phenomenon.

(21) Appl. No.: **13/776,801**

(22) Filed: **Feb. 26, 2013**

(30) **Foreign Application Priority Data**

Oct. 29, 2012 (KR) 10-2012-0120646

Publication Classification

(51) **Int. Cl.**
G09G 3/32 (2006.01)

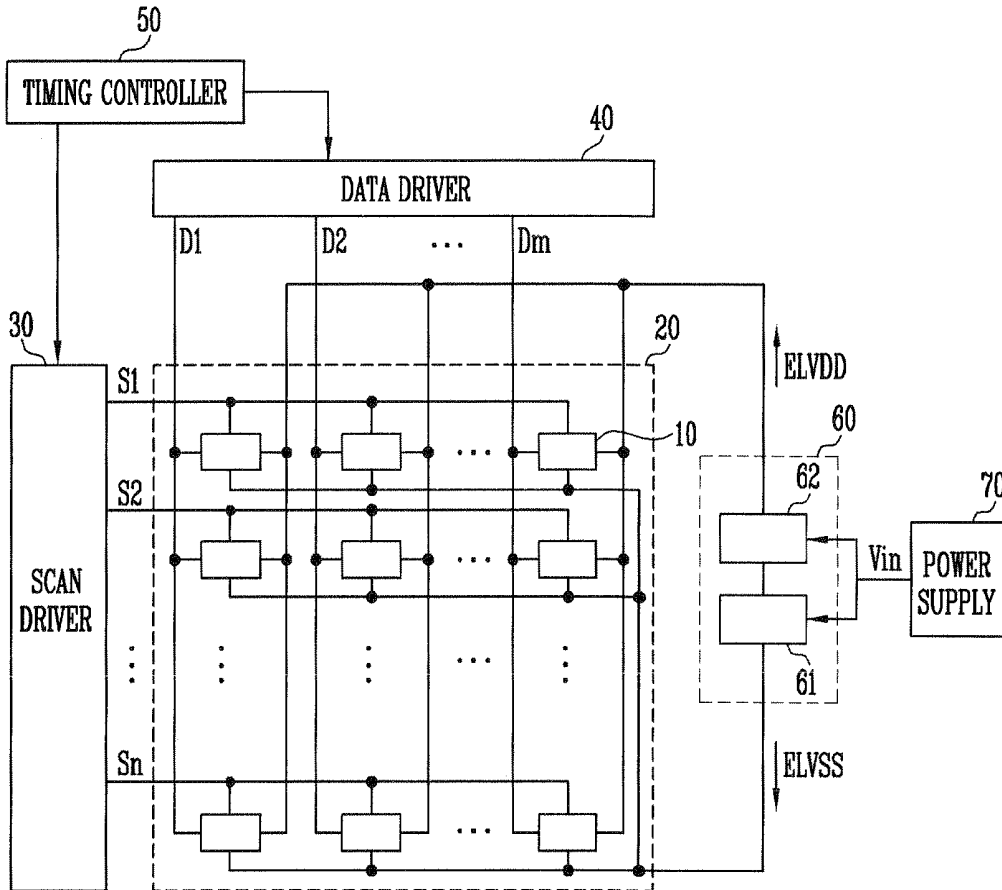


FIG. 1

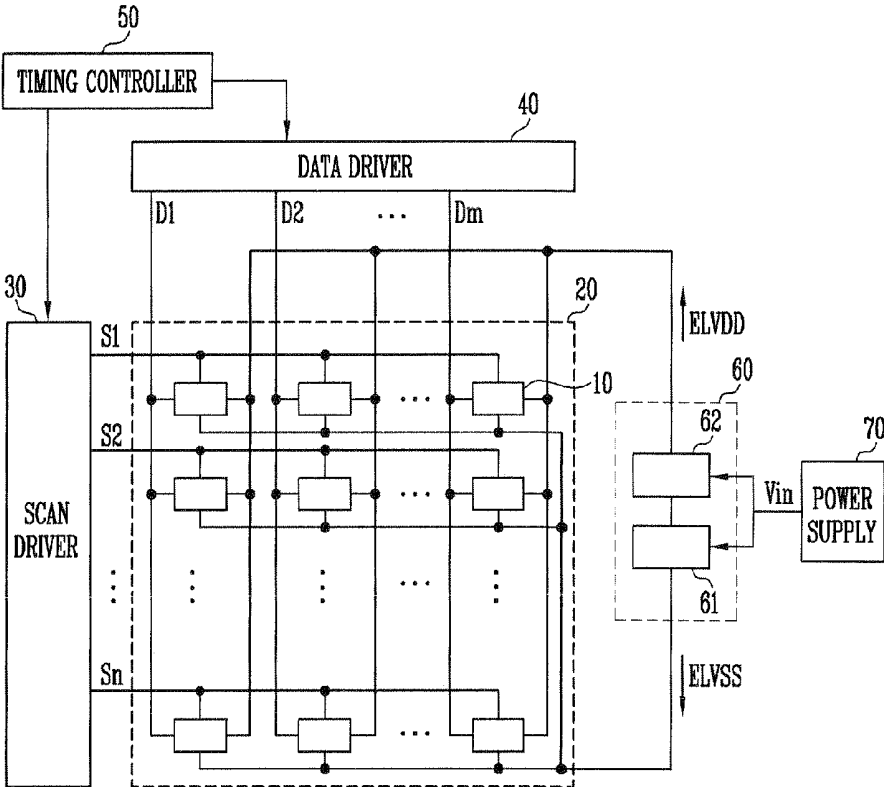


FIG. 2

10

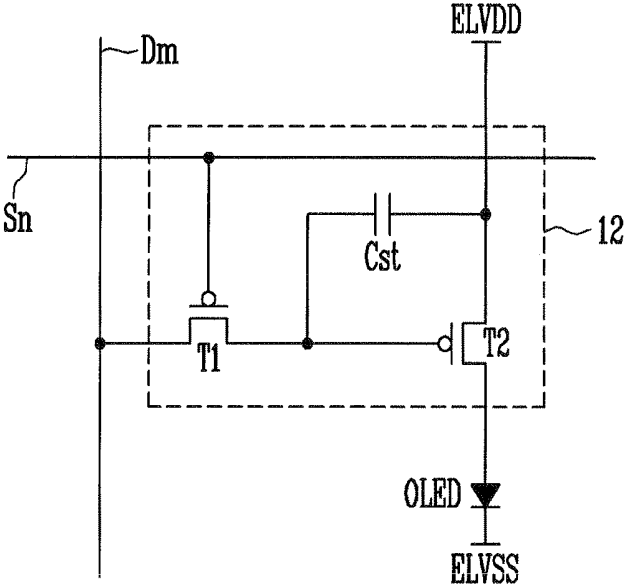
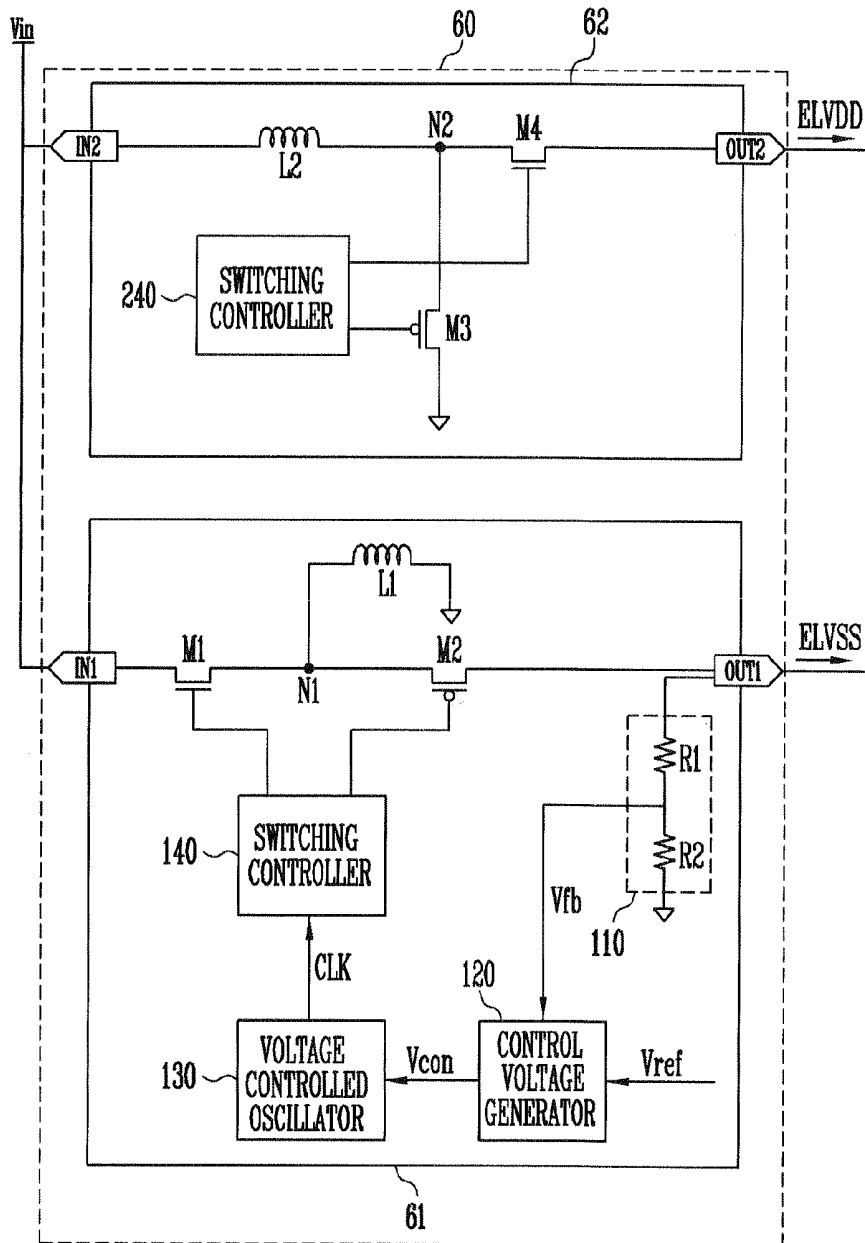


FIG. 3



ORGANIC LIGHT EMITTING DISPLAY

CLAIM OF PRIORITY

[0001] This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C. §119 from an application earlier filed in the Korean Intellectual Property Office on the 29 Oct. 2012 and there duly assigned Serial No. 10-2012-0120646.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to an organic light emitting display, and more particularly, to an organic light emitting display which can improve power conversion efficiency and reduce a flicker phenomenon.

[0004] 2. Description of the Related Art

[0005] Recently, there have been developed various types of displays capable of reducing the weight and volume of cathode ray tubes, which are disadvantages. The displays include a liquid crystal display (LCD), a field emission display (FED), a plasma display panel (PDP), an organic light emitting display (OLED), etc.

[0006] Among these displays, the organic light emitting display displays images using organic light emitting diodes that emit light through recombination of electrons and holes. The organic light emitting display has a fast response speed and is driven with low power consumption.

[0007] The organic light emitting display includes a power supply that generates and supplies voltages required to drive the organic light emitting display through conversion of external power.

[0008] Generally, a switching regulator for DC-DC conversion is widely used as the power supply of the organic light emitting display.

[0009] As the organic light emitting display is employed in a mobile device, etc., interest in power conversion efficiency of the power supply increases.

[0010] However, there is a problem in that, although the switching frequency of the switching regulator has great influence on the power conversion efficiency of the power supply, the organic light emitting display of the related art is used by fixing the switching frequency of the switching regulator, regardless of load capacity.

[0011] Furthermore, as the scan frequency of a scan driver is set without considering the switching frequency of the switching regulator, a flicker phenomenon may occur on a screen.

SUMMARY OF THE INVENTION

[0012] The present invention relates to an organic light emitting display which can improve power conversion efficiency and reduce a flicker phenomenon.

[0013] According to an aspect of the present invention, there is provided an organic light emitting display, including: a plurality of pixels coupled to scan lines and data lines; a scan driver that supplies a scan signal to the pixels through the scan lines according to a predetermined scan frequency; a data driver that supplies a data signal to the pixels through the data lines; and a first switching regulator that supplies a first voltage to the pixels and has a changeable switching frequency, the switching frequency of the first switching regulator being changed while avoiding the scan frequency of the scan driver.

[0014] The switching frequency of the first switching regulator may be changed while avoiding the scan frequency and a harmonic frequency of the scan frequency.

[0015] The first switching regulator may include: a first switching element coupled between a first node and a first input terminal through which an input voltage is applied to the first switching element; a second switching element coupled between the first node and a first output terminal through which the first voltage is outputted; a first inductor coupled between the first node and a ground; and a first switching controller that controls the first and second switching elements according to the switching frequency.

[0016] The first switching controller may change the switching frequency by reflecting the first voltage.

[0017] The first switching regulator may further include: a control voltage generator that generates a control voltage using the difference between a reference voltage and a feedback voltage reflecting the first voltage; and a voltage controlled oscillator that generates a clock signal having a frequency changed depending on the control voltage.

[0018] The first switching controller may control the switching frequency in synchronization with the frequency of the clock signal supplied from the voltage controlled oscillator.

[0019] The first switching regulator may further include a voltage divider that generates the feedback voltage by dividing the first voltage of the first output terminal.

[0020] The first and second switch elements may be implemented as transistors.

[0021] The first voltage may be a negative voltage.

[0022] The first and second switching elements may be alternately turned on.

[0023] The organic light emitting display may further include a second switching regulator that supplies a second voltage to the pixels.

[0024] The second switching regulator may include: a second inductor coupled between a second node and a second input terminal through which the input voltage is applied to the second inductor; a third switching element coupled between the second node and the ground; a fourth switching element coupled between the second node and a second output terminal through which the second voltage is outputted; and a second switching controller that controls the third and fourth switching elements.

[0025] The third and fourth switching elements may be implemented as transistors.

[0026] The third and fourth switching elements may be alternately turned on.

[0027] As described above, according to the present invention, it is possible to provide an organic light emitting display which can improve power conversion efficiency and reduce a flicker phenomenon.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings, in which like reference symbols indicate the same or similar components, wherein:

[0029] FIG. 1 is a block diagram illustrating an organic light emitting display according to an embodiment of the present invention.

[0030] FIG. 2 is a circuit diagram illustrating an embodiment of a pixel shown in FIG. 1.

[0031] FIG. 3 is a circuit diagram illustrating a power supply according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0032] Hereinafter, certain exemplary embodiments according to the present invention will be described with reference to the accompanying drawings. Here, when a first element is described as being coupled to a second element, the first element may not only be directly coupled to the second element but may also be indirectly coupled to the second element via a third element. Furthermore, some of the elements that are not essential to a complete understanding of the invention are omitted for clarity. Also, like reference numerals refer to like elements throughout.

[0033] Hereinafter, an organic light emitting display according to an embodiment of the present invention will be described in detail with reference to the accompanying drawings.

[0034] FIG. 1 is a block diagram illustrating an organic light emitting display according to an embodiment of the present invention.

[0035] Referring to FIG. 1, the organic light emitting display according to this embodiment includes a pixel unit 20 having a plurality of pixels 10 coupled to scan lines S_1 to S_n and data lines D_1 to D_m , a scan driver 30 that supplies a scan signal to each pixel 10 through the scan lines S_1 to S_n , a data driver 40 that supplies a data signal to each pixel 10 through the data lines D_1 to D_m , and a power supply 60 that supplies a first voltage ELVSS and a second voltage ELVDD to each pixel 10. The organic light emitting display may further include a timing controller 50 that controls the scan driver 30 and the data driver 40.

[0036] Each pixel 10 that receives the first and second voltages ELVSS and ELVDD, respectively, from the power supply 60 may emit light corresponding to a data signal by current flowing from the second voltage ELVDD to the first voltage ELVSS via the organic light emitting diode OLED.

[0037] The scan driver 30 generates a scan signal under the control of the timing controller 50, and supplies the generated scan signal to the scan lines S_1 and S_n .

[0038] In this case, the scan driver 30 may supply the scan signal according to a predetermined scan frequency.

[0039] For example, the number of scan lines in an HD or WXGA organic light emitting display is 1280. Thus, in a case where 60 frames are displayed for 1 second, the scan frequency can be set to 76.8 kHz.

[0040] The scan frequency of the scan driver 30 may be controlled by the timing controller 50.

[0041] The data driver 40 generates a data signal under the control of the timing controller 50, and supplies the generated data signal to the data lines D_1 to D_m .

[0042] If a scan signal is sequentially supplied to the scan lines S_1 to S_n , pixels 10 are sequentially selected for each line. Thus, the selected pixels 10 can receive a data signal supplied from the data lines D_1 to D_m .

[0043] FIG. 2 is a circuit diagram illustrating an embodiment of a pixel shown in FIG. 1. Particularly, for convenience of illustration, a pixel coupled to an n -th scan line S_n and an m -th scan line D_m is shown in FIG. 2.

[0044] Referring to FIG. 2, the pixel 10 includes an organic light emitting diode OLED and a pixel circuit 12 coupled to

the data line D_m and the scan line S_n so as to control the organic light emitting diode OLED.

[0045] An anode electrode of the organic light emitting diode OLED is coupled to the pixel circuit 12, and a cathode electrode of the organic light emitting diode OLED is coupled to the first voltage ELVSS.

[0046] The organic light emitting diode OLED generates light with a predetermined luminance, corresponding to current supplied from the pixel circuit 12.

[0047] The pixel circuit 12 controls the amount of current supplied to the organic light emitting diode OLED, corresponding to a data signal supplied to the data line D_m when a scan signal is supplied to the scan line S_n . To this end, the pixel circuit 12 includes a second transistor T2 coupled between the second voltage ELVDD and the organic light emitting diode OLED, a first transistor T1 coupled among the second transistor T2, the data line D_m and the scan line S_n , and a storage capacitor Cst coupled between a gate electrode and a first electrode of the second transistor T2.

[0048] A gate electrode of the first transistor T1 is coupled to the scan line S_n , and a first electrode of the first transistor T1 is coupled to the data line D_m .

[0049] A second electrode of the first transistor T1 is coupled to one terminal of the storage capacitor Cst.

[0050] Here, the first electrode is set as any one of source and drain electrodes, and the second electrode is set as an electrode different from the first electrode. For example, if the first electrode is set as a source electrode, the second electrode is set as a drain electrode.

[0051] The first transistor T1 coupled to the scan line S_n and the data line D_m is turned on when a scan signal is supplied from the scan line S_n , so as to supply a data signal supplied from the data line D_m to the storage capacitor Cst.

[0052] The gate electrode of the second transistor T2 is coupled to the one terminal of the storage capacitor Cst, and the first electrode of the second transistor T2 is coupled to the other terminal of the storage capacitor Cst. A second electrode of the second transistor T2 is coupled to the anode electrode of the organic light emitting diode OLED.

[0053] The second transistor T2 controls the amount of current flowing from the second voltage ELVDD to the first voltage ELVSS via the organic light emitting diode OLED, corresponding to the voltage stored in the storage capacitor Cst. In this case, the organic light emitting diode OLED emits light corresponding to the amount of the current supplied from the second transistor T2.

[0054] The pixel structure of FIG. 2 described above is merely an embodiment of the present invention, and therefore, the pixel 10 of the present invention is not limited to the pixel structure. Practically, the pixel circuit 12 has a circuit structure capable of supplying current to the organic light emitting diode OLED, and the circuit structure may be selected as any one of various circuit structures currently known in the art.

[0055] The power supply 60 of FIG. 1 generates the first and second voltages ELVSS and ELVDD supplied to each pixel 10 by receiving an input voltage V_{in} inputted from the power supply 70 and converting the input voltage V_{in} .

[0056] Preferably, the first voltage ELVSS is set as a negative voltage, and the second voltage ELVDD is set as a positive voltage.

[0057] The power supply 70 may be a battery for providing DC voltage or a rectifier for converting AC voltage into DC

voltage and outputting the DC voltage. However, the present invention is not limited thereto.

[0058] FIG. 3 is a circuit diagram illustrating a power supply according to an embodiment of the present invention.

[0059] Referring to FIGS. 1 and 3, the power supply 60 according to this embodiment may include a first switching regulator 61 that generates the first voltage ELVSS from the input voltage V_{in} , and a second switching regulator 62 that generates the second voltage ELVDD from the input voltage V_{in} .

[0060] The first switching regulator 61 converts the input voltage V_{in} into the first voltage ELVSS, and supplies the first ELVSS to each pixel 10.

[0061] In this case, the switching frequency of the first switching regulator 61 is not fixed to a specific frequency but may be changed.

[0062] For example, the first switching regulator 61 may change the switching frequency according to the capacity of a load in order to improve power conversion efficiency.

[0063] In a case where the switching frequency of the first switching regulator 61 corresponds to the scan frequency of the scan driver 30, a flicker phenomenon may occur on a screen. Therefore, the switching frequency of the first switching regulator 61 is preferably changed while avoiding the scan frequency of the scan driver 30.

[0064] In order to more radically remove the flicker phenomenon, the switching frequency of the first switching regulator 61 is preferably set so as not to overlap with a harmonic frequency of the scan frequency.

[0065] For example, when the scan frequency of the scan driver 30 is 76.8 kHz, a second harmonic frequency of the scan frequency may be obtained as 153.6 kHz, and a third harmonic frequency of the scan frequency may be obtained as 230.4 kHz.

[0066] Therefore, the switching frequency of the first switching regulator 61 is preferably changed while avoiding not only the scan frequency of the scan driver 30 but also the harmonic frequency of the scan frequency.

[0067] For example, the switch frequency of the first switching regulator 61 may be changed into 50 kHz, 100 kHz, 200 kHz, etc. so as not to overlap with the scan frequency and the harmonic frequency.

[0068] In this case, information on the scan frequency of the scan driver 30 may be provided from the timing controller 50 to the first switching regulator 61.

[0069] Referring to FIG. 3, the first switching regulator 61 may include a first switching element M1, a second switching element M2, a first inductor L1 and a first switching controller 140.

[0070] The first switching element M1 may be coupled between a first node N1 and a first input terminal IN1 through which the input voltage V_{in} is applied to the first switching element M1.

[0071] The second switching element M2 may be coupled between the first node N1 and a first output terminal OUT1 through which the first voltage ELVSS is outputted.

[0072] The first inductor L1 may be coupled between the first node N1 and a ground.

[0073] In this case, the first node N1 may be defined as a common node of the first switching element M1, the second switching element M2 and the first inductor L1.

[0074] The first switching controller 140 may control the first and second switching elements M1 and M2, respectively.

[0075] Particularly, the first switching controller 140 controls on/off operations of the first and second switching elements M1 and M2, respectively, according to the switching frequency, so that the input voltage V_{in} can be converted into the first voltage ELVSS having a desired voltage level.

[0076] In this case, the first and second switching elements M1 and M2, respectively, may be alternately turned on.

[0077] The first and second switching elements M1 and M2, respectively, may be implemented as transistors.

[0078] The first and second switching elements M1 and M2, respectively, may be implemented as transistors having different conductive types for convenience of controlling the transistors. For example, in a case where the first switching element M1 is implemented as an n-type transistor, the second switching element M2 may be implemented as a p-type transistor.

[0079] The first switching controller 140 may change the switching frequency by reflecting the first voltage ELVSS outputted through the first output terminal OUT1.

[0080] For example, in a case where the amplitude of the first voltage ELVSS increases, the first switching controller 140 may increase the switching frequency by deciding that the capacity of the load increases.

[0081] In a case where the amplitude of the first voltage ELVSS decreases, the first switching controller 140 may decrease the switching frequency by deciding that the capacity of the load decreases.

[0082] To this end, the first switching regulator 61 may further include a control voltage generator 120 and a voltage controlled oscillator 130.

[0083] The control voltage generator 120 may generate a control voltage V_{con} , using the difference between a feedback voltage V_{fb} reflecting the first voltage ELVSS and a reference voltage V_{ref} .

[0084] The control voltage generator 120 may supply the generated control voltage V_{con} to the voltage controlled oscillator 130.

[0085] In this case, the level of the control voltage V_{con} may be changed depending on the difference of the feedback voltage V_{fb} reflecting the first voltage ELVSS and the reference voltage V_{ref} .

[0086] The feedback voltage V_{fb} may be generated from a voltage divider 110 that divides the first voltage ELVSS of the first output terminal OUT1.

[0087] The voltage divider 110 may be configured with a plurality of resistors R1 and R2 coupled to the first output terminal OUT1.

[0088] The voltage controlled oscillator 130 generates a clock signal CLK having a frequency changed depending on the control voltage V_{con} supplied from the control voltage generator 120, and supplies the generated clock signal CLK to the first switching controller 140.

[0089] That is, the frequency of the clock signal CLK may be changed depending on the level of the control voltage V_{con} .

[0090] The frequency of the clock signal CLK is changed while avoiding the scan frequency of the scan driver 30 and the harmonic frequency of the scan frequency.

[0091] In this case, the first switching controller 140 that receives the clock signal CLK may control the switching frequency in synchronization of the frequency of the clock signal CLK.

[0092] Thus, the switching frequency of the first switching regulator 61 can be synchronized with the frequency of the clock signal CLK.

[0093] As a result, the switching frequency can be changed depending on the capacity of the load through the configuration described above, thereby increasing the power conversion efficiency of the first switching regulator 61.

[0094] Furthermore, the scan frequency of the scan driver 30 and the harmonic frequency of the scan frequency can be avoided, thereby reducing the flicker phenomenon.

[0095] The second switching regulator 62 converts the input voltage V_{in} into the second voltage ELVDD, and supplies the second voltage ELVDD to each pixel 10.

[0096] Referring to FIG. 3, the second switching regulator 62 may include a second inductor L2, a third switching element M3, a fourth switching element M4 and a second switching controller 240.

[0097] The second inductor L2 may be coupled between a second node N2 and a second input terminal IN2 through which the input voltage V_{in} is applied to the second inductor L2.

[0098] The third switching element M3 may be coupled between the second node N2 and the ground.

[0099] The fourth switching element M4 may be coupled between the second node N2 and a second output terminal OUT2 through which the second voltage ELVDD is output.

[0100] In this case, the second node N2 may be defined as a common node of the second inductor L2, the third switching element M3 and the fourth switching element M4.

[0101] The second switching controller 240 may control the third and fourth switching elements M3 and M4.

[0102] The second switching controller 240 controls on/off operations of the third and fourth switching elements M3 and M4, so as to convert the input voltage V_{in} into the second voltage ELVDD having a desired voltage level.

[0103] In this case, the third and fourth switching elements M3 and M4 may be alternately turned on.

[0104] The third and fourth switching elements M3 and M4 may be implemented as transistors.

[0105] The third and fourth switching elements M3 and M4 may be implemented as transistors having different conductive types for convenience of controlling the transistors. For example, in a case where the third switching element M3 is implemented as a p-type transistor, the fourth switching element M4 may be implemented as an n-type transistor.

[0106] While the present invention has been described in connection with certain exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims, and equivalents thereof.

What is claimed is:

1. An organic light emitting display, comprising:

- a plurality of pixels coupled to scan lines and data lines;
- a scan driver that supplies a scan signal to the pixels through the scan lines according to a predetermined scan frequency;
- a data driver that supplies a data signal to the pixels through the data lines; and
- a first switching regulator that supplies a first voltage to the pixels and has a changeable switching frequency;

the switching frequency of the first switching regulator being changed while avoiding the scan frequency of the scan driver.

2. The organic light emitting display according to claim 1, the switching frequency of the first switching regulator being changed while avoiding the scan frequency and a harmonic frequency of the scan frequency.

3. The organic light emitting display according to claim 1, the first switching regulator comprising:

- a first switching element coupled between a first node and a first input terminal through which an input voltage is applied to the first switching element;
- a second switching element coupled between the first node and a first output terminal through which the first voltage is outputted;
- a first inductor coupled between the first node and a ground; and
- a first switching controller that controls the first and second switching elements according to the switching frequency.

4. The organic light emitting display according to claim 3, the switching controller changing the switching frequency by reflecting the first voltage.

5. The organic light emitting display according to claim 4, the first switching regulator further comprising:

- a control voltage generator that generates a control voltage using the difference between a reference voltage and a feedback voltage reflecting the first voltage; and
- a voltage controlled oscillator that generates a clock signal having a frequency changed depending on the control voltage.

6. The organic light emitting display according to claim 5, the first switching controller controlling the switching frequency in synchronization with the frequency of the clock signal supplied from the voltage controlled oscillator.

7. The organic light emitting display according to claim 5, the first switching regulator further comprising a voltage divider that generates the feedback voltage by dividing the first voltage of the first output terminal.

8. The organic light emitting display according to claim 3, the first and second switching elements being implemented as transistors.

9. The organic light emitting display according to claim 1, the first voltage being a negative voltage.

10. The organic light emitting display according to claim 3, the first and second switching elements being alternately turned on.

11. The organic light emitting display according to claim 1, further comprising a second switching regulator that supplies a second voltage to the pixels.

12. The organic light emitting display according to claim 11, the second switching regulator comprising:

- a second inductor coupled between a second node and a second input terminal through which the input voltage is applied to the second inductor;
- a third switching element coupled between the second node and the ground;
- a fourth switching element coupled between the second node and a second output terminal through which the second voltage is outputted; and
- a second switching controller that controls the third and fourth switching elements.

13. The organic light emitting display according to claim 12, the third and fourth switching elements being implemented as transistors.

14. The organic light emitting display according to claim 12, the third and fourth switching elements being alternately turned on.

* * * * *

专利名称(译)	有机发光显示器		
公开(公告)号	US20140118323A1	公开(公告)日	2014-05-01
申请号	US13/776801	申请日	2013-02-26
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO., LTD.		
[标]发明人	PARK SUNG CHEON		
发明人	PARK, SUNG-CHEON		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3291 G09G3/3233 G09G2300/0828 G09G2300/0842 G09G2320/0247 G09G2330/00		
优先权	1020120120646 2012-10-29 KR		
外部链接	Espacenet USPTO		

摘要(译)

一种有机发光显示器，包括：多个像素，耦合到扫描线和数据线；扫描驱动器，根据预定的扫描频率通过扫描线向像素提供扫描信号；数据驱动器，通过数据线向像素提供数据信号；第一开关调节器，向像素提供第一电压并具有可变的开关频率。在有机发光显示器中，改变第一开关调节器的开关频率，同时避免扫描驱动器的扫描频率。因此，可以提供一种有机发光显示器，其可以提高功率转换效率并减少闪烁现象。

